SCS:lam 10/3/02 144712
PATENT

Attorney Reference Number 6319-56134
Application Number 09/660,753

REMARKS

1. Claims 1, 2, 3, 5, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, and 20 were amended in applicant's communication filed May 13, 2002, in response to the first Office action dated February 13, 2002.

2. The first Office action dated February 13, 2002 was traversed in applicant's communication filed May 13, 2002, in response to the first Office action dated February 13, 2002.

3. Applicant appreciates the Examiner's review of his first response (filed September 3, 2002) to the Office action (final rejection) dated July 3, 2002.

4. Applicant also appreciates the Examiner's Advisory Action dated September 18, 2002, and respectfully requests reconsideration in light of the foregoing amendments and the following remarks.

5. Both claims 1 and 11 have been amended to state "the second surface has no electrical connection device thereon" and "etching said semiconductor unit from said second surface to reduce semiconductor unit volume". Claim 19 has been amended to state "the second surface has no electrical connection device thereon" and "applying beams of light on said second surface to reduce die volume," as well as "the first surface is shielded by the seating apparatus from the beams of light". Allowance of amended claims 1, 11, and 19 is respectfully requested in view of the foregoing amendments and the following remarks. Original claims 2, 3, 4, 5, 6, 7, 8, 9, and 10 ultimately depend on amended claim 1, original claims 12, 13, 14, 15, 16, 17, and 18 ultimately depend on amended claim 11, and original claim 20 ultimately depends on amended claim 19, and therefore are considered to be in condition for allowance.

6. All features added to claims 1, 11 and 19 are supported generally by the specification

and drawings of the present application as a whole, and particularly by lines 20-28 on page 7, lines 5-15 on page 9, lines 13-15 on page 7, lines 12-21 on page 8, and Figs. 1-8, and 10-15.

7. The amendments of claims 1, 11, and 19 were made to further clarify distinctions between the claimed invention and the subject matter disclosed by Dery *et al.*, Hudak *et al.*, and Siniaguine.

The present application is in condition for allowance, and such action is requested.

Applicant also would like to thank Examiner Vinh for the courtesy of the telephone interview with the undersigned on October 3, 2002. During this telephone conference, Examiner Vinh agreed to call the undersigned to discuss the Amendment, unless Examiner Vinh passes the application to allowance.

Respectfully submitted,
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Marked-up Version of Amended Claims
Pursuant to 37 C.F.R. §§ 1.121(b)-(c)

In the Claims

1. (Amended) A method for reducing the size of at least a semiconductor unit in a process of making a package including a carrier and said semiconductor unit, said semiconductor unit including a first surface and a second surface, said second surface having no electrical connection device thereon, said method comprising the steps of:

attaching at least a part of said first surface to said carrier; and

etching said semiconductor unit from said second surface to reduce semiconductor unit volume until the size of said semiconductor unit meets an expected specification.

11. (Amended) A method for reducing the size of at least a semiconductor unit in a process of lead-on-chip packaging wherein said semiconductor unit includes a first surface[,] and a second surface, [and] said first surface having at least an electrical connection device thereon [located on said first surface], said second surface having no electrical connection device thereon, said method comprising the steps of:

attaching said semiconductor unit to a chip carrier in such a way that said semiconductor unit and said chip carrier are in a configuration of lead-on-chip, with said first surface facing said chip carrier and said second surface exposed; and

etching said semiconductor unit from said second surface to reduce semiconductor unit volume until the size of said semiconductor unit meets an expected specification.

19. (Amended) A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a

second surface, and at least an electrical connection device located on said first surface, said method comprising the steps of:

dividing a wafer into a plurality of dice;

placing at least one die of said dice onto a seating apparatus, with said second surface exposed;

applying beams of light on said second surface to reduce die volume[etch said dice], with said first surface shielded by said seating apparatus [and thereby immunized against etching] from said beams of light.